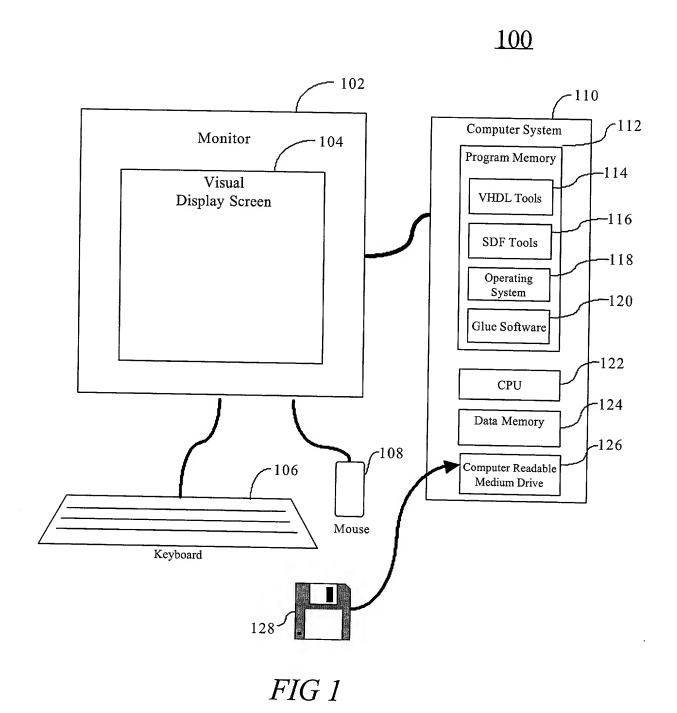
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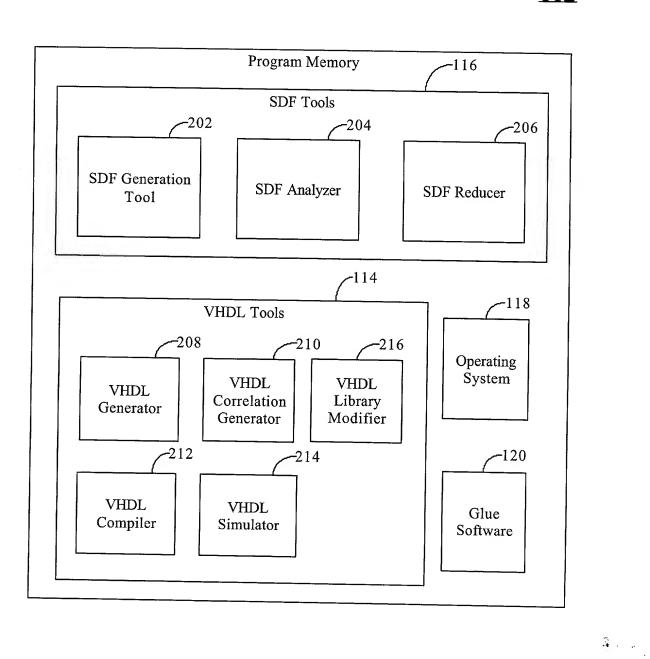


FIG 2

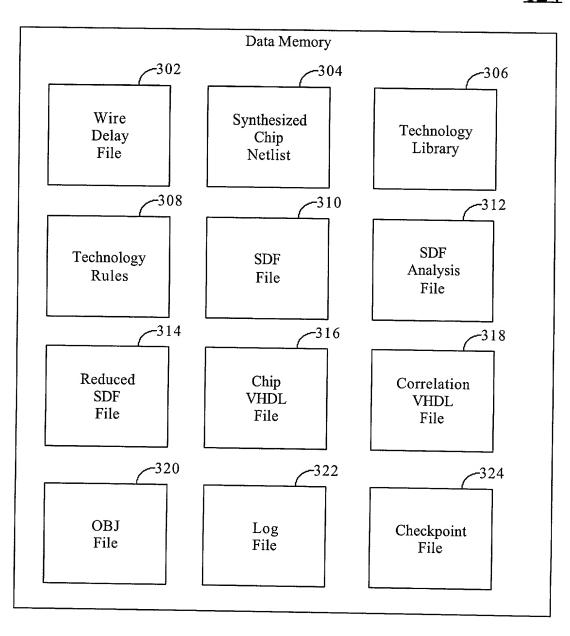


FIG 3

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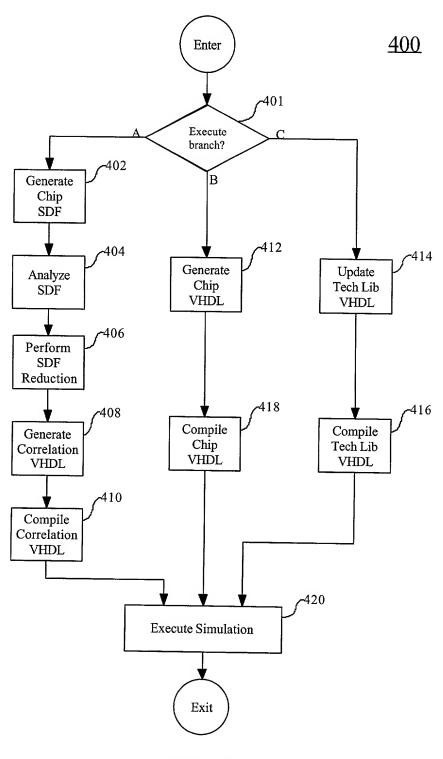


FIG 4

ary to ,

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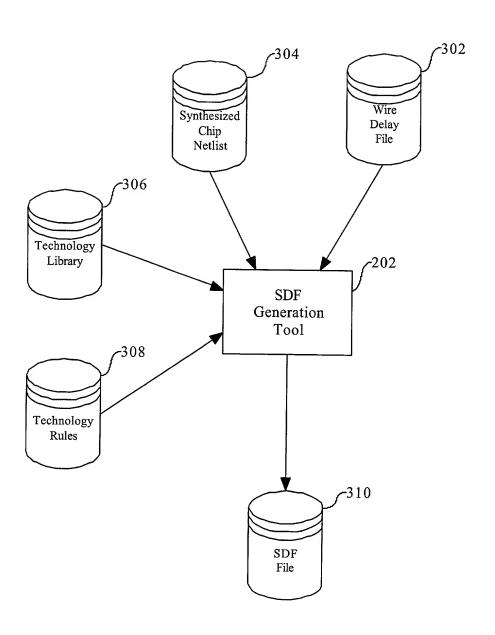


FIG 5

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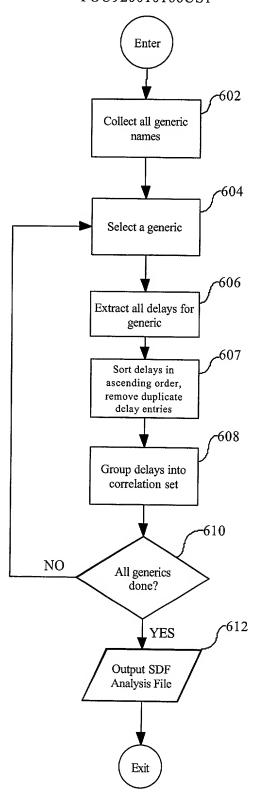


FIG 6

17.1

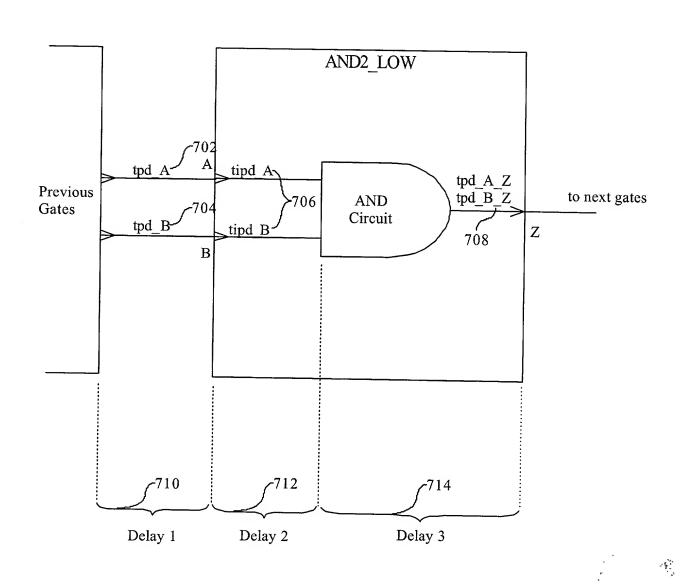


FIG 7

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<u>800</u>

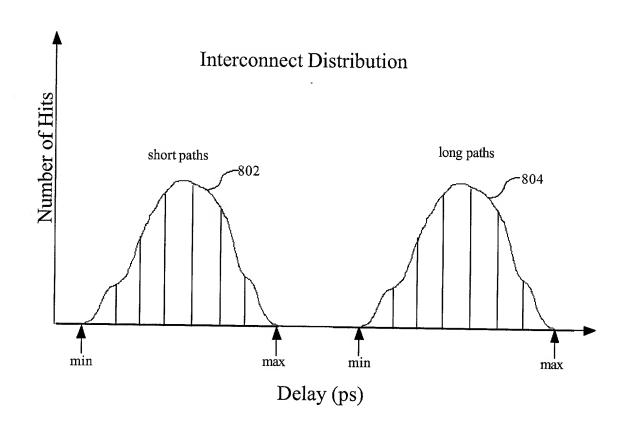


FIG 8

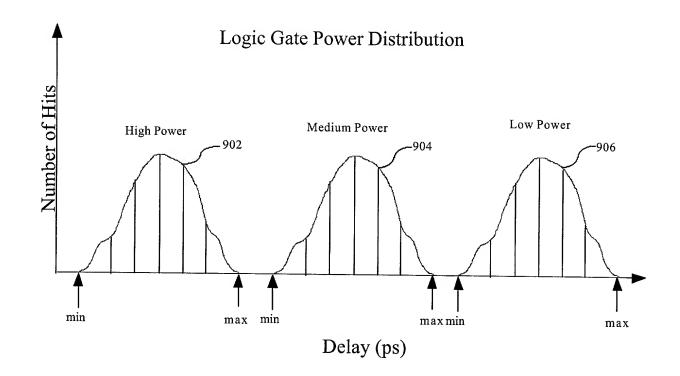


FIG 9

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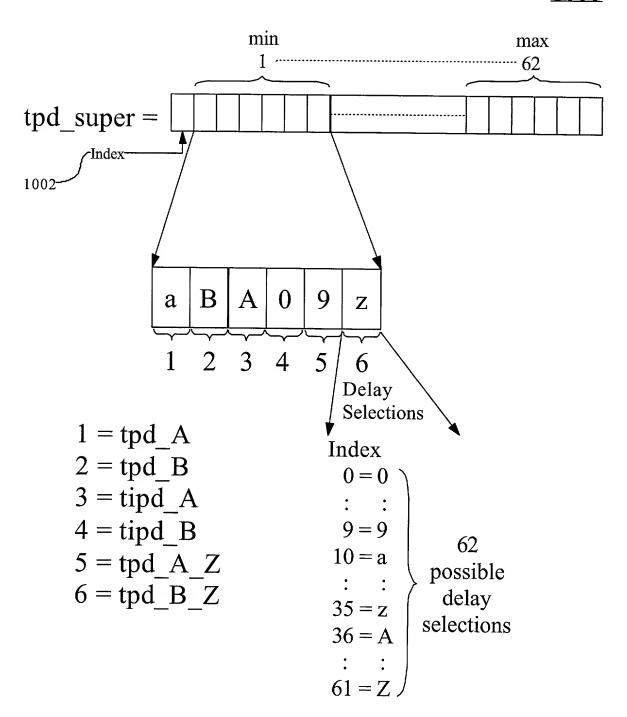


FIG 10

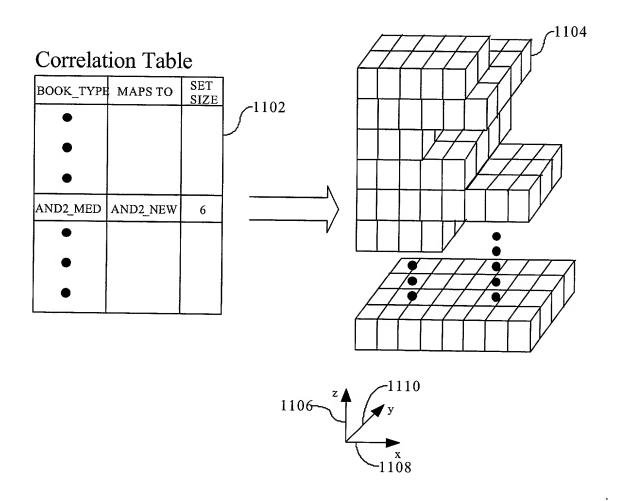


FIG 11

1200

CHAR POSITION (0 OFFSET)	CHAR VALUE	Correlation Set (x')	Entry Position (y')	Slot Offset (x")
0	1	N/A	N/A	N/A
1	4	1	5th	1st
2	X	1	60th	2nd
3	a	1	11th	3rd
4	m	1	26th	4th
5	р	1	29th	5th
6		1	25th	6th

FIG 12



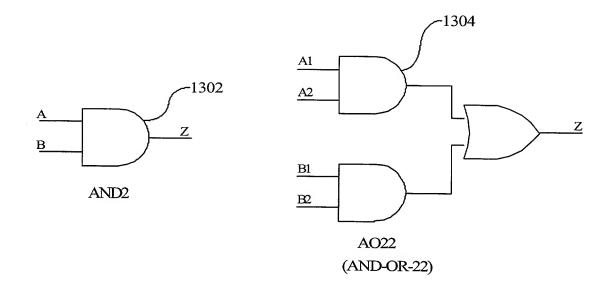


FIG 13

1400

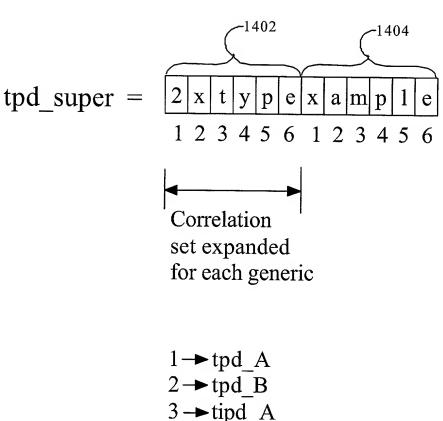


FIG 14

15.18

1500

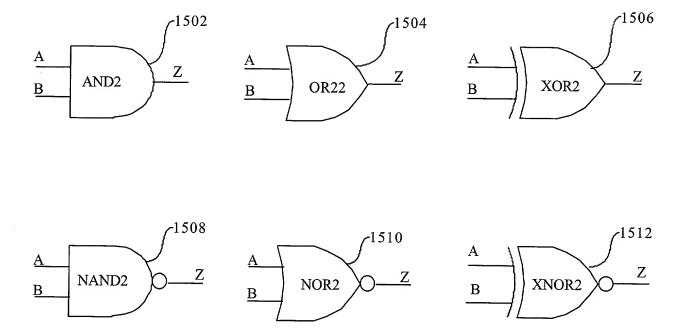
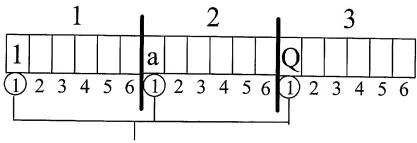


FIG 15

. .

1600



tpd_A positions for AND2 gate

Encode as:

DELAY		tpd A	
DELAY	1	2	3
	0	0	0
-0.499 ns	0	0	1
ر <u>•</u> ا	_ •	<i>-</i>	k • 4
• -	•		<u> </u>
+237.826 ns	Z	Z	Υ
+237.827 ns	Z	Z	Z
	DELAY -0.500 ns -0.499 ns +237.826 ns +237.827 ns	DELAY 1 -0.500 ns 0 -0.499 ns 0 +237.826 ns Z	DELAY 1 2 -0.500 ns 0 0 -0.499 ns 0 0 +237.826 ns Z Z

FIG 16

4.

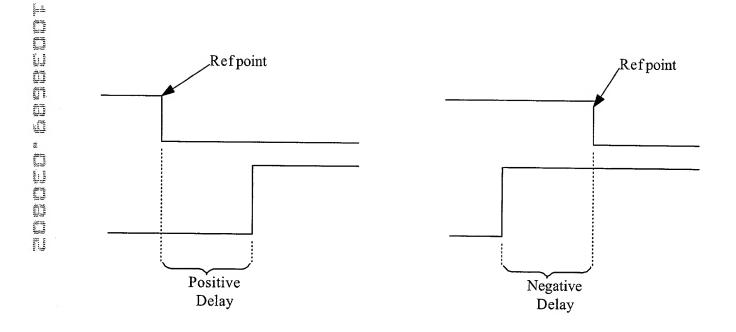


FIG 17

<u>406</u>

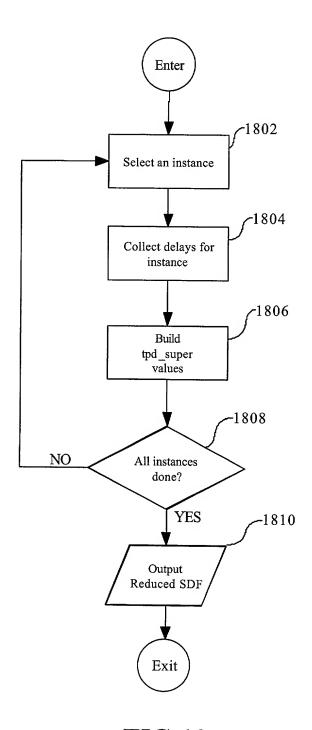


FIG 18

<u>408</u>

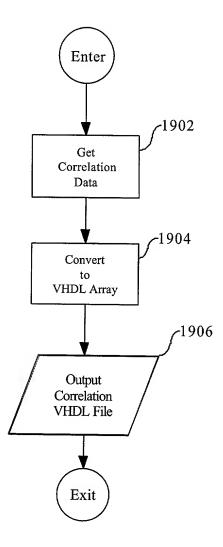


FIG 19

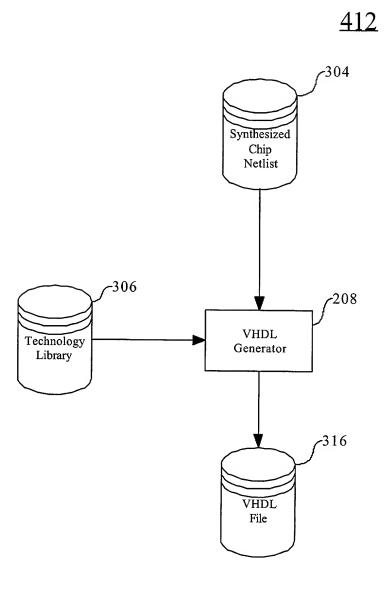


FIG 20

<u>418</u>

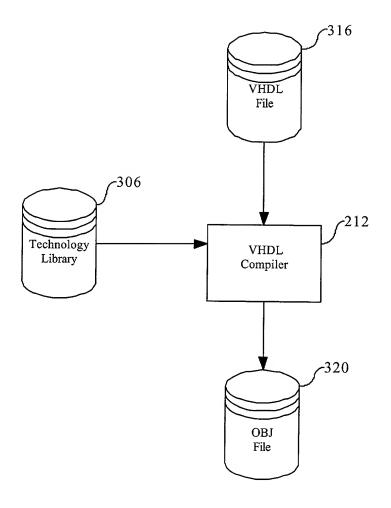


FIG 21

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<u>420</u>

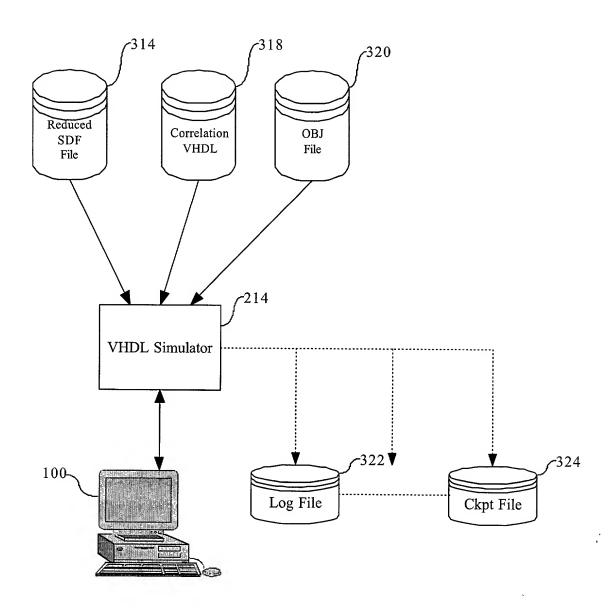


FIG 22